

Appl. No. 10/695,976
 Amdt. dated July 13, 2006
 Reply to Office Action of June 7, 2006

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

- 1 Claim 1. (currently amended) A method comprising:
 2 receiving a serial stream of data bits;
 3 deserializing the serial stream of data bits into parallel bits;
 4 inputting the parallel bits into a content addressable memory and a first register;
 5 inputting an output of the first register into a second register;
 6 inputting outputs of the first and second registers to the content addressable
 7 memory;
 8 providing a bus configured to receive the parallel bits and output of the first
 9 register, wherein the data lines forming the bus are grouped into a plurality of overlapping
 10 subsets of the bus that each contain at least one common data line;
 11 providing the parallel bits and the output of the first register in a plurality of
 12 parallel bit outputs formats onto the bus; and
 13 selecting one of the subsets and associated parallel bit outputs ~~formats to output~~
 14 based on match flag outputs from the content addressable memory, wherein the match flag
 15 outputs are generated in response to the inputs to the content addressable memory.
- 1 Claim 2. (currently amended) The method of claim 1 wherein the plurality of
 2 parallel bits and the output of the first register ~~output formats~~ are input to a plurality of tristate
 3 driver circuits, and wherein selecting one of the subsets and the associated parallel bit outputs
 4 ~~formats to output~~ comprises:
 5 enabling one of the tristate driver circuits to output the parallel bits and the output
 6 of the first register ~~output format~~ associated with that tristate driver ~~circuits~~ circuit to an output
 7 bus, and disabling other ones of the tristate driver circuits coupled to the output bus.
- 1 Claim 3. (original) The method of claim 1 wherein there are eight parallel bits.

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1 Claim 4. (original) The method of claim 1 wherein the first and second registers
2 are two stages of a shift register.

1 Claim 5. (original) The method of claim 1 wherein a depth of the content
2 addressable memory comprises at least one row for each of the parallel bits.

1 Claim 6. (original) The method of claim 1 wherein the inputs to the content
2 addressable memory are provided by way of parallel transfer.

1 Claim 7. (original) The method of claim 6 wherein a width of the parallel bits
2 inputting the content addressable memory is at least a number of parallel bits output from the
3 deserializer plus a length of a pattern to be detected using the content addressable memory minus
4 1.

1 Claim 8. (currently amended) A circuit comprising:
2 a deserializer circuit coupled to receive serial data input and outputting a first
3 parallel data output, wherein the deserializer circuit outputs the first parallel data onto a bus
4 that is configured with overlapping subsets of the bus, wherein the subsets include at least one
5 common data line;
6 a shift register coupled to the first parallel data output; and
7 a content addressable memory, coupled to the shift register to receive the first
8 parallel data output in parallel.

1 Claim 9. (currently amended) The circuit of claim 8 further comprising:
2 a plurality of second parallel data outputs ~~formats~~ based on the first parallel data
3 output, wherein each of second parallel data outputs are associated with a respective one of the
4 subsets; and
5 a plurality of tristate buffer circuits, one coupled to each of the subsets of the bus
6 ~~parallel data output formats.~~

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1 Claim 10. (original) The circuit of claim 9 further comprising:
2 a control logic block, coupled to a match signal from the content addressable
3 memory, generating a plurality of select signals, one coupled to each of the tristate buffer
4 circuits.

1 Claim 11. (original) The circuit of claim 10 wherein based on the match signal,
2 the control logic block generates select signals to enable one of the tristate buffers and disable
3 others of the tristate buffers.

1 Claim 12. (original) The circuit of claim 10 wherein the control logic block
2 comprises a state machine.

1 Claim 13. (currently amended) The circuit of claim 9 wherein there is one
2 parallel data output ~~format~~ for each bit of the first parallel data output minus 1.

1 Claim 14. (original) The circuit of claim 8 wherein the shift register is divided
2 into three portions, the first portion of the shift register is coupled to the deserializer, the second
3 portion of the shift register is coupled to the first portion through a first multiplexer, and the third
4 portion of the shift register is coupled to the second portion through a second multiplexer.

1 Claim 15. (currently amended) The circuit of claim 14 wherein the third portion
2 ~~position~~ of the shift register is coupled to the first portion of the shift register through the second
3 multiplexer.

1 Claim 16. (currently amended) The circuit of claim 14 wherein the second
2 portion ~~position~~ of the shift register is coupled to the deserializer through the first multiplexer.

1 Claim 17. (original) The circuit of claim 8 wherein each row in the content
2 addressable memory comprises a data pattern to be detected in the serial data input.

1 Claim 18. (original) The circuit of claim 8 wherein the content addressable
2 memory has a number of rows equal to or greater than a number of bits of the first parallel data
3 output.

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1 Claim 19. (original) The circuit of claim 8 wherein the content addressable
2 memory comprises a bit pattern comprising "1111," "0110," "0010," and "1000" in at least a
3 number of rows that is equal to a number of bits of the first parallel data output.

1 Claim 20. (original) The circuit of claim 8 wherein the first parallel data output
2 is 8, 10, 16, or 20 bits wide.

1 Claim 21. (original) A programmable logic integrated circuit comprising the
2 circuit of claim 8.

1 Claim 22. (original) The circuit of claim 8 further comprising:
2 a plurality of parallel data output formats based on the first parallel data output;
3 and
4 a selector circuit, coupled to each of the parallel data output formats and the first
5 parallel data output, outputting one of the parallel data output formats as a second parallel data
6 output based on an output from the content addressable memory.

1 Claim 23. (original) The circuit of claim 8 wherein the first parallel data output
2 comprises 8 bits in a format bit 0, bit 1, bit 2, bit 3, bit 4, bit 5, bit 6, and bit 7, and the circuit
3 further comprises:
4 a first parallel data output format comprising bit 1, bit 2, bit 3, bit 4, bit 5, bit 6,
5 bit 7, and bit 0;
6 a second parallel data output format comprising bit 2, bit 3, bit 4, bit 5, bit 6, bit 7,
7 bit 0, and bit 1; and
8 a third parallel data output format comprising bit 3, bit 4, bit 5, bit 6, bit 7, bit 0,
9 bit 1 and bit 2;
10 a fourth parallel data output format comprising bit 4, bit 5, bit 6, bit 7, bit 0, bit 1,
11 bit 2, and bit 3;
12 a fifth parallel data output format comprising bit 5, bit 6, bit 7, bit 0, bit 1, bit 2,
13 bit 3, and bit 4;
14 a sixth parallel data output format comprising bit 6, bit 7, bit 0, bit 1, bit 2, bit 3,
15 bit 4, and bit 5; and

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16 a seventh parallel data output format comprising bit 7, bit 0, bit 1, bit 2, bit 3, bit
17 4, bit 5, and bit 6.

1 Claim 24. (previously presented) A method comprising:
2 deserializing an input serial data stream into a first parallel word;
3 generating a second parallel word from the first parallel word;
4 grouping the second parallel word into a plurality of data word subsets that
5 overlap to include at least one common data bit;
6 generating a third parallel word from the first and second parallel word; and
7 detecting a frame alignment symbol within the third parallel word by comparing a
8 bit pattern of the third parallel word to a plurality of frame alignment patterns stored in a content
9 addressable memory.

1 Claim 25. (previously presented) The method of claim 24, further comprising
2 selecting one of the subsets associated with a respective one of the frame alignment patterns that
3 matches the frame alignment symbol.

1 Claim 26. (previously presented) The method of claim 24, wherein detecting the
2 frame alignment symbol comprises detecting the frame alignment symbol within one clock
3 cycle.

1 Claim 27. (previously presented) The method of claim 24, wherein grouping the
2 second parallel word comprises outputting the second parallel word on a data bus that includes
3 subsets of data lines that correspond to the data word subsets.